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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/617,441	07/14/2000	HIROTAKA KAWATA	106310	5358

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	#12

DATE MAILED: 03/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/617,441	KAWATA, HIROTAKA	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. This application contains claims 9 – 19 drawn to an invention nonelected with traverse in Paper No. 7. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to clearly show how the gate electrodes extend in both a width and length direction as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the gate-length and gate width must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3 - 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakazawa et al. (USPAT 5614730, Nakazawa).

Nakazawa discloses in figures 19a – 19c and 20 an electro-optical device. Nakazawa discloses in figures 19a – 19c and 20 a substrate (109). Nakazawa discloses in figures 19a – 19c and 20 a plurality of scanning lines (101) provided on the substrate. Nakazawa discloses in figures 19a – 19c and 20 a plurality of data lines (108) crossing the plurality of scanning lines. Nakazawa discloses in figures 19a – 19c and 20 a plurality of transistors formed with gate electrodes (113) having ends in a gate-width direction and ends in a gate-length direction, each transistor being connected (1906 and 1904, respectively) to one of the scanning lines and one of the data lines. Nakazawa discloses in figures 19a – 19c and 20 pixel electrodes (107) connected (1905) to the transistors. Nakazawa discloses in figures 19a – 19c and 20 at least one portion of the ends in the gate-width direction of the gate electrodes forming the transistors being disposed in a semiconductor region (102) forming the transistor, and the ends in the gate-length direction of each of the gate electrodes extending outside of the semiconductor region forming the transistor.

With regard to claim 3, Nakazawa discloses in column 4, lines 3 – 12 the semiconductor region forming the transistor comprises polycrystalline silicon.

With regard to claim 4, Nakazawa discloses in column 3, line 57 the substrate being an insulative substance.

With regard to claim 5, Nakazawa discloses in column 3, line 57 the substrate being an quartz substrate.

With regard to claim 6, Nakazawa discloses in column 3, line 57 the substrate being an glass substrate.

With regard to claim 7, Nakazawa discloses in figure 23b a second substrate (313) disposed opposing a surface of the first substrate. Nakazawa discloses in figure 23b liquid crystals (312) sandwiched by the first substrate and the second substrate, and driven by transistor elements formed on the semiconductor layers.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of one of ordinary skill in the art.

Nakazawa does not disclose the semiconductor region forming the transistor comprises monocrystalline silicon. Monocrystalline silicon is a well known material to form a semiconductor region with. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use monocrystalline silicon as the semiconductor for the transistor of Nakazawa in order to improve the channel characteristics.

With regard to claim 8, it has been held in In re Pearson 181 USPQ 641 (CCPA) that intended use does not avoid prior art. Therefore, it would have been obvious to use the device of claim 1 as an LCD projector.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of Nishihara et al. (JPPAT 06163891, Nishihara).

Nakazawa does not teach that portions of the plurality of scanning lines form the gate electrodes. Nishihara teaches in figures 7 and 8 portions of a scanning line (5) form gate electrode. (it is inherent that there would be a plurality of both scanning lines and gate electrodes in Nishihara. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the portion of the scanning lines as part of the gate electrodes of Nishihara in the device of Nakazawa in order to decrease the cost of manufacturing the device by decreasing the number of masking steps needed.

Response to Arguments

9. Applicant's arguments filed January 18, 2002 have been fully considered but they are not persuasive.

10. With regard to the applicant's argument that "according to the active matrix substrate of Nakazawa et al., the one end in the gate width direction of the gate electrodes are disposed outside of the semiconductor region and the end in the gate length direction of the gate electrodes are arranged inside of the semiconductor region," is not persuasive. It should be noted that the definition of which direction the gate length is arranged is derived from the applicant's own specification on page 10, lines 8 – 10 where the applicant states that "the gate-length direction is a direction in which the data line 6a extends, and the gate –width direction is a direction perpendicular to the gate-length direction." It should be noted that in figure 19a of Nakazawa the gate-length direction is a direction in which the data line 108 extends. It can therefore be determined that Nakazawa discloses in figures 19a – 19c and 20 at least one portion of the ends in the gate-width direction of the gate electrodes forming the transistors being disposed in a semiconductor region (102) forming the transistor, and the ends in the gate-length direction of each of the gate electrodes extending outside of the semiconductor region forming the transistor, and the rejection is proper.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 21, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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